



Australian
National
University

Venue _____

Student Number

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School of Computing

EXAMINATION

Semester 1 - In-Class, 2026

COMP2300/COMP6300/ENGN2219_Semester 1 Computer Architecture

This paper is for ANU, ANU and ANU students.

Examination Duration: 90 minutes

Reading Time: 0 minutes

Exam Conditions:

90 mins

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

No materials permitted

Materials To Be Supplied To Students:

Scribble Paper x 2

Instructions To Students: The exam is marked out of 100. There are six questions. Each question has multiple sub-questions. The mark for each question is indicated in the table below.

Question 1	30	
Question 2	18	
Question 3	12	
Question 4	12	
Question 5	10	
Question 6	18	
Total	100	

Question 1: Multiple choice and true/false questions [+2 for correct, -1 for wrong, 0 for no selection]. Write your choice of answer in the table below.

a	b	c	d	e	f	g	h	i	j	k	l	m	n	o

a. The number of bits needed to represent -128 in 2's complement number system:

- A. 7
- B. 8
- C. 9
- D. 10
- E. None of the above

b. The expression $ABC + A'BC + AB'C$ is equivalent to:

- A. $ABC + BC$
- B. $C(A + B)$
- C. ABC
- D. $AB + BC$
- E. $ABC + B'C$

c. A logic gate with two inputs, A and B, outputs B when A is Logic 0, and the complement of B, when A is Logic 1. Which logic gate is it?

- A. OR
- B. AND
- C. XOR
- D. XNOR
- E. NAND

d. Under De Morgan's Theorem, which of the following circuits are equivalent:

- A. An AND gate with inverted output *is equivalent to* an AND gate with inverted inputs
- B. An AND gate with inverted output *is equivalent to* a NOR gate with inverted output
- C. An AND gate with inverted output *is equivalent to* an XOR gate with inverted inputs
- D. An OR gate with inverted output *is equivalent to* an OR gate with inverted inputs
- E. A NOR gate with inverted output *is equivalent to* an AND gate with inverted inputs
- F. None of the above

e. A 2:4 decoder can be used to implement an XOR gate by connecting which ones of its one-hot outputs to the inputs of an OR gate:

- A. 00 and 01
- B. 00 and 11
- C. 01 and 10
- D. 10 and 11
- E. 00 and 10

f. Which of the following statements correctly describes the internal architecture of a Programmable Logic Array (PLA)?

- A. It consists of a fixed AND plane followed by a programmable OR plane.
- B. It consists of a programmable AND plane followed by a programmable OR plane.
- C. It uses a decoder to select a single word line which then drives a fixed OR plane.
- D. It consists of a programmable AND plane followed by a fixed OR plane.
- E. It is a purely sequential circuit that uses a clock signal to synchronize the AND and OR planes.

g. A memory array that uses a 2:4 decoder to store 1-byte words has an address space (in bits) of:

- A. 16
- B. 32
- C. 64
- D. 128
- E. 256

h. When the addressability of memory is increased from 8 to 32 bits without changing the number of locations (rows):

- A. The complexity of decoding logic reduces
- B. The complexity of decoding logic increases
- C. The complexity of decoding logic stays the same
- D. None of the above

i. Which of the following is not true about synchronous sequential circuits according to the standard composition rules?

- A. Every circuit element must be either a register or a combinational element
- B. Every cyclic path in the circuit must contain at least one register
- C. All registers in the system must receive the same clock signal
- D. A circuit is considered synchronous even if it consists entirely of combinational logic elements
- E. All races are eliminated if the clock is slow enough to allow inputs to all registers to settle before the next clock edge

j. Which of the following does not impact code density?

- A. The choice between fixed-length and variable-length instruction encoding
- B. The number of programmer-visible registers
- C. The sophistication of memory addressing modes (e.g., base + offset)
- D. The clock frequency of the processor
- E. The availability of complex instructions (CISC vs. RISC)

k. The width of architectural registers in a CPU is determined by:

- A. ISA
- B. Microarchitecture
- C. None of the above

l. The decision to place the PC inside or outside the register file is determined by:

- A. ISA
- B. Microarchitecture
- C. None of the above

m. The clock frequency of a CPU is determined by:

- A. ISA
- B. Microarchitecture
- C. None of the above

n. The number of ALUs in a CPU is determined by:

- A. ISA
- B. Microarchitecture
- C. None of the above

o. Which of the following impact the execution time of a program?

- A. The average number of cycles per instruction (CPI)
- B. The clock frequency of the processor
- C. The strength of the compiler's optimization passes
- D. The number of instructions in the compiled binary
- E. The sophistication of the compiler's register allocation algorithm
- F. All of the above

Question 2: A priority encoder has 2^N inputs. It produces an N-bit binary output indicating the most significant bit of the input that is TRUE. It also produces an output NONE that is TRUE if none of the inputs are TRUE. Design an eight-input priority encoder with inputs $A_{7:0}$ and outputs $Y_{2:0}$ and NONE.

For example:

If the input is 00100000, the output Y should be 101 and NONE should be 0.

Answer the following three parts. You may use the white space on the next page if needed.

- A. Draw the truth table for the combinational logic of the priority encoder. Use don't-care to simplify the table.

- B. Give a simplified Boolean equation for each output using the sum-of-products (SOP) form. Show how each expression is obtained from the truth table.

- C. Using only basic logic gates (AND, OR, NOT), draw a logic diagram (schematic) of the priority encoder. Clearly label all inputs and outputs. You can use logic gates with more than two inputs.

Question 3: Design an SR latch with NAND gates only. Describe the behavior of the latch for each of the four input combinations. Discuss one specific case in detail.

A. Latch Schematic

B. Behaviour

You can use Q and Q' in the output columns to refer to the previously latched value.

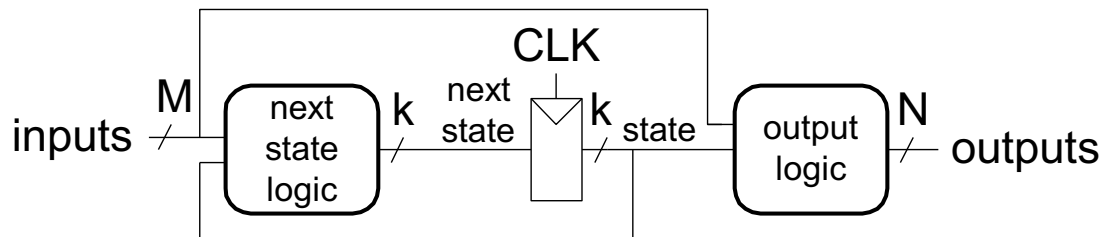
R	S	Q	Q'

C. Discuss in detail the behaviour of the latch when $R = 0$, $S = 0$.

Question 4: Consider memory storage of a 32-bit word stored at memory word 42 in a byte-addressable memory.

- A. What is the byte address of memory word 42?
- B. What are the byte addresses that memory word 42 spans?
- C. Draw the number 0xFF223344 stored at word 42 in both big-endian and little-endian machines. Clearly label the byte address corresponding to each byte value.

Question 5: The following high-level synchronous sequential circuit consists of combinational next state logic with M-bit input, a K-bit register, and N-bit output logic.



Timing specification

- The clock-to-Q propagation delay (t_{pcq}) is equal to 0.3 nanoseconds.
- The setup time (t_{setup}) is equal to 0.1 nanoseconds.
- The hold time (t_{hold}) is zero.
- Assume wires have no delay.
- The critical path of the next state logic has a total delay of 1.2 nanoseconds.

A. What type of circuit does the above block diagram represent? Briefly explain what the above circuit does.

B. What is the maximum clock frequency at which a circuit designer can operate the circuit?

Question 6: Consider the following high-level code snippet. Assume the signed integer variables *g* and *h* are in registers *R0* and *R1*, respectively. Answer the three questions below.

```
if (g >= h)
    g = g + h;
else
    g = g - h;
```

- A. Write the code snippet in ARM assembly language assuming conditional execution is available for branch instructions only. Use as few instructions as possible.
- B. Write the code snippet in ARM assembly language with conditional execution available for all instructions. Use as few instructions as possible.

- C. Compare the difference in code density (i.e., number of instructions) between (A) and (B) for each code snippet and discuss any advantages or disadvantages.