ENGN2219/COMP6719 Computer Systems & Organization Problem Set 4

Note: This problem set is optional for your practice only and not part of the assessment scheme.

Question 1:

Explain the difference between a latch and a flip-flop? Under what circumstances is each one preferable?

Question 2:

Explain the concept of pipelining, and what is the prime benefit of pipelining.

Question 3:

In the context of a flip-flop, explain the key difference between setup time and hold time.

Question 4:

Explain the key disadvantages of asynchronous sequential circuits. Why are synchronous sequential circuits preferred over asynchronous ones?

Question 5:

Consider the following 3-stage pipelined circuit. Each box labeled CL is a combinational block. The propagation delay of each CL block is listed in the figure (pink). Assume the setup time is 0.45 ns, and the clock-to-Q propagation delay is 0.5 ns. Assume the hold time is negligible.



A) What is the end-to-end latency of finishing one task using the pipelined circuit above?

B) Find the (maximum) clock frequency at which it is safe to operate the pipeline?

C) Suppose CL4 can be further pipelined into two stages that each take 3 ns. Find the new end-to-end latency of performing a single task. What is the new clock frequency?

Question 6:

Give three examples from the QuAC architecture of each of the architecture design principles: (1) regularity supports simplicity; (2) make the common case fast; (3) smaller is faster; and (4) good design demands good compromises. Explain how each of your examples exhibits the design principle.

Question 7:

Consider the following microarchitecture of the ARM ISA we have seen in lectures.



For the instruction, STR R0, [R1, #12], find the values of all the control signals in blue. Use the lecture slides or textbook or any other material as your aid.

Question 8:

Explain the purpose of the two adders in the figure in Question 7. Also, explain the need for each of the multiplexers in the same figure.