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Minimizing Bank Selection Instructions for Partitioned Memory Architectures

Resource constraints are a major concern with the design, development, and deployment of embedded systems. Bank switching is a technique that increases the code and data memory in microcontrollers without extending the address buses. Given a program in which variables have been assigned to data banks, we present a novel optimization technique that minimizes the overhead of bank switching through cost-effective placement of bank selection instructions. The optimal placement is controlled by a variety of different objectives, such as runtime, low power, small code size or a combination of these parameters. We have formulated the problem as a form of Partitioned Boolean Quadratic Programming (PBQP).

We conducted experiments for a variety of embedded systems benchmarks, such as MiBench, DSPStone, and an embedded systems real-time kernel. Our optimization achieved a reduction of program memory space between 2.7% and 18.2%, and an overall performance improvement between 5.1% and 28.8%. Our optimization achieved an optimal solution for all benchmark programs.